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# THD Analysis of Carrier Overlapping PWM Strategies for DCMI With Reduced Number Of Switches

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**ABSTRACT**: This paper presents a three level, five and nine level diode clamped multilevel inverter topology with reduced number of switches which can be used for low-medium power drive applications. The diode clamped multi-level inverter topology is very promising in ac drives, when both reduced harmonic contents & high power are required. The reduction in the number of switches, cost and complexity of the circuit makes it suitable for various application. It can offer a low total harmonic distortion and high efficiency.

**KEYWORDS:** Diode clamp multilevel inverter, Reduced number of switches, Total harmonic distortion

## I. INTRODUCTION

Recently, single-phase induction motor is widely used in buildings and industries because of its compact size, endurance and cheap price.. In this paper, the concept of a 3,5,9-level diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible. Therefore, controlling approach of voltage and frequency supplied to stator coil in order to control the motor speed efficiently according to actual operations which was developed by [1-2] is employed. New diode clamping multilevel inverter. Developed DC link capacitor voltage balancing in a three phase diode clamped inverter controlled by a direct space vector of line to line voltages. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

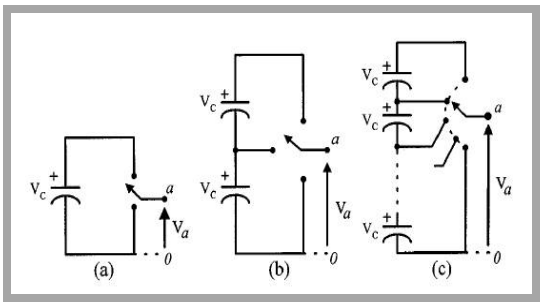


Figure 1: One Phase Leg Of An Inverter With (A) Two Levels, (B) Three Levels, And (C) N Levels

## II. SYSTEM MODEL AND ASSUMPTIONS

It considers a network with N mobile unlicensed nodes that move in an environment according to some stochastic mobility models. It also assumes that entire spectrum is divided into number of M non-overlapping orthogonal channels having different bandwidth. The access to each licensed channel is regulated by fixed duration time slots. Slot timing is assumed to be broadcast by the primary system. Before transmitting its message, each transmitter node, which is a node with the message, first selects a path node and a frequency channel to copy the message. After the path and channel selection, the transmitter node negotiates and handshakes with its path node and declares the selected channel frequency to the path. The communication needed for this coordination is assumed to be accomplished by a fixed length frequency hopping sequence (FHS) that is composed of K distinct licensed channels. In each time slot, each node consecutively hops on FHS within a given order to transmit and receive a coordination packet. The aim of

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coordination packet that is generated by a node with message is to inform its path about the frequency channel decided for the message copying.

As in the single phase voltage source inverters PWM technique can be used in three-phase inverters, in which three sine waves phase shifted by 120° with the frequency of the desired output voltage is compared with a very high frequency carrier triangle, the two signals are mixed in a comparator whose output is high when the sine wave is greater than the triangle and the comparator output is low when the sine wave or typically called the modulation signal is smaller than the triangle. This phenomenon is shown in Fig. 2. As is explained the output voltage from the inverter is not smooth but is a discrete waveform and so it is more likely than the output wave consists of harmonics, which are not usually desirable since they deteriorate the performance of the load, to which these voltages are applied

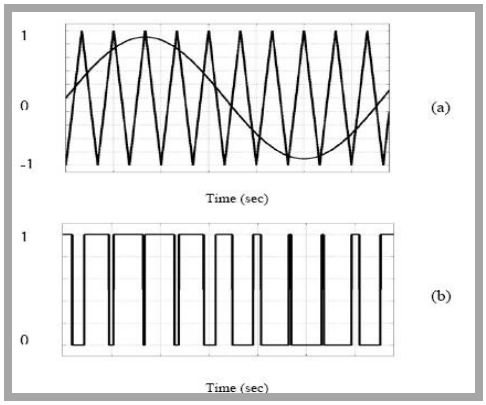


Figure 2: PWM Illustration by the Sine-Triangle Comparison (a) Sine-Triangle Comparison (b) Switching Pulses

## III. MULTI LEVEL INVERTER TOPOLOGY

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load.

The main multilevel topologies are classified into three categories:

- diode clamped inverters
- flying capacitor inverters
- cascaded inverters

In a three-phase inverter system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure.

The diode-clamp inverter type is used for experimentations in this article. Such inverter employs the technique of proportional stepping harmonic elimination type to control switching equipment in the circuit for providing appropriated waveform and increasing the efficiency at high loading.

## IV. DIODE-CLAMPED MULTILEVEL INVERTER

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is Vdc. An n level inverter needs (n-1) voltage sources, 2(n-1) switching devices and (n-1) (n-2) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform.

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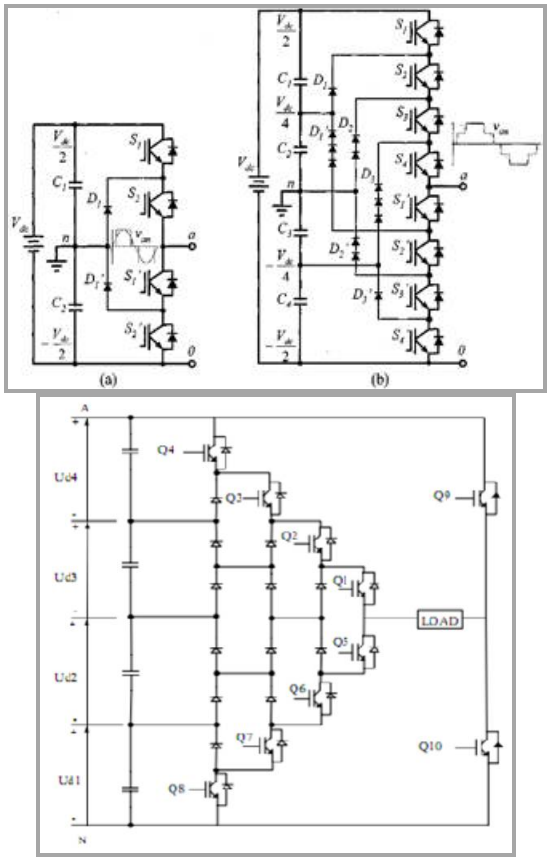


Figure 3: Diode-Clamped Multilevel Inverter Circuit Topologies. (a) Three-level (b) Five-level (c) Nine-level

Figure.3(a) shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, $C_1$, $C_2$. For dc-bus voltage $V_{dc}$, the voltage across each capacitor is $V_{dc}/2$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/2$ through clamping diodes. The order of numbering of the switches for phase a is $S_1$, $S_2$, $S_1'$ and $S_2'$ . To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. If switching sequence as given in table 1. State condition 1 means switch ON and 0 means switch OFF.

| $V_0$ | $S_1$ | $S_2$ | $S_1'$ | $S_2'$ |
|---|---|---|---|---|
| $V_{dc}/2$ | 1 | 1 | 0 | 0 |
| **0** | 0 | 1 | 1 | 0 |
| $-V_{dc}/2$ | 0 | 0 | 1 | 1 |

Table1: The switching states of a 3-level diode clamped multilevel inverter.

There are three switch combinations to synthesize three-level voltages across a and n.

1. Voltage level $V_{an}= V_{dc}/2$, turn on the switches $S_1$and$S_2$.
2. Voltage level $V_{an}= 0$, turn on the switches $S_2$ and $S_1'$.
3. Voltage level $V_{an}= - V_{dc}/2$ turn on the switches $S_1'$, $S_2'$.

Figure.3 (b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, $C_1$, $C_2$, $C_3$, and $C_4$. For dc-bus voltage $V_{dc}$, the voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to

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one capacitor voltage level $V_{dc}/4$ through clamping diodes. The order of numbering of the switches for phase a is $S_1$, $S_2$, $S_3$, $S_4$, $S_1'$, $S_2'$, $S_3'$ and $S_4'$.
For example to have $V_{dc}/2$ in the output, switches $S_1$ to $S_4$ should conduct at the same time. For each voltage level four switches should conduct. As it can be seen in Table.1 the maximum output voltage in the output is half of the DC source. It is a drawback of the diode clamped multilevel inverter. This problem can be solved by using a two times voltage source or cascading two diode clamped multilevel inverters. The output voltage of a 5-level diode clamped multilevel inverter all of the voltage level should have the same voltage value.
The switching angles should be calculated in such a way that the THD of the output voltage becomes as low as possible. The switching angle calculation method that is used in this thesis is the harmonic elimination method. In this method the lower dominant harmonics can be eliminated by choosing calculated switching angles. Table-1 shows the output voltage levels and the corresponding switch states for one phase of the chosen five level DCMLI. The switches are arranged into 4 pairs ($S_1$, $S_1'$), ($S_2$, $S_2'$), ($S_3$, $S_3'$), ($S_4$, $S_4'$). If switching sequence as given in table 2. State condition 1 means switch ON and 0 means switch OFF.

| $V_0$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_1'$ | $S_2'$ | $S_3'$ | $S_4'$ |
|---|---|---|---|---|---|---|---|---|
| $V_{dc}/2$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $V_{dc}/4$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| **0** | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $-V_{dc}/4$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| $-V_{dc}/2$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

Table2: The switching states of a 5-level diode clamped multilevel inverter

The steps to synthesis the five level phase a output voltage in this work are as follows:
1. For phase a output voltage of $V_{an}=0$, two upper switches $S_3$, $S_4$ and two lower switches $S_1'$ and $S_2'$ are turned on.
2. For an output voltage of $V_{an}=V_{dc}/4$, three upper switches $S_2$, $S_3$, $S_4$ and one lower switch $S_1'$ are turned on.
3. For an output voltage of $V_{an}=V_{dc}/2$, all upper switches $S_1$ through $S_4$ are turned on.
4. To obtain the output voltage of $V_{an}= -V_{dc}/4$, upper switch $S_4$ and three lower switches $S_1'$, $S_2'$ and $S_3'$ are turned on.
5. For an output voltage of $V_{an} = -V_{dc}/2$, all lower switches $S_1'$ through $S_4'$ are turned on.
The phase a output voltage Van has five states: $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$. The gate signals for the chosen five level DCMLI are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. Diode clamped multilevel inverter is a very general and widely used topology. DCMLI works on the concept of using diodes to limit voltage stress on power devices.

### 3. Reduced Switching Topology

For practical implementation, the switching state needs to be converted into transistor signals. Once the transistor signals are established, general expressions for the a-phase line to ground voltage & the a-phase component of the DC currents can be written as

$$V_{ao}= H_{an}V_{n0}+ H_{an-1}V_{n-10}+\ldots..+H_{a1}V_{10} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

$$V_{bo}= H_{bn}V_{n0}+ H_{bn-1}V_{n-10}+\ldots..+H_{b1V10} \quad \ldots\ldots\ldots\ldots\ldots (2)$$

$$V_{co}= H_{cn}V_{n0}+ H_{cn}\text{-}1V_{n-10}+\ldots..+H_{c1V10} \quad \ldots\ldots\ldots\ldots\ldots (3)$$

The Node Currents for the "n" level inverter are given by

$$I_n = H_{an}I_a+H_{bn}I_b+H_{cn}I_c$$

$$I_{n-1} = (H_{an-1})I_a+(H_{bn-1})I_b+(H_{cn-1})I_c$$

$$I_1 = H_{a1}I_a+H_{b1}I_b+H_{c1}I_c \quad \ldots\ldots\ldots\ldots\ldots (4)$$

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The above relationships may be programmed into simulation software that simulates one phase of a diode clamped inverter. A number of blocks can be connected together for a multiphase system. For more simulation details, the transistor & diode KCL & KVL equations may be implemented. This allows inclusion of the device voltage drops & also the individual device voltages & currents.
To express this relationship, consider the general N level diode clamped structure. Through the clamping action of diodes, the blocking voltage of each transistor is the corresponding capacitor voltage in the series bank. Finally the capacitor junction currents may be expressed as the difference of two clamping diode currents. In case of a three level inverter, the expression reduces to

$C_{1p}V_{c1} = -(I_{dc}+H_{a3}I_a+H_{b3}I_b+H_{c3}I_c)$ ..... (5)

$C_{1p}V_{c2} = -(I_{dc}+H_{a1}Ia+H_{b1}I_b+H_{c1}I_c)$ ..... (6)

**Total Harmonic Distortion (THD) Calculation**

As introduced in the first chapter, the total harmonics distortion (THD) is mathematically given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^{\,2}}}{H_1}$$

where $H_1$ is the amplitudes of the fundamental component, whose frequency is w0 and Hn is the amplitudes of the nth harmonics at frequency nw0. The amplitude of the fundamental and harmonic components of the quarter-wave symmetric multilevel waveform can be express as:
Therefore,

$$h_n = \frac{4E}{n\pi}\sum_{k=1}^{S}\cos(n\alpha_k)$$

let $H_{(n)} = h_n$ and $H_1 = h_1$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} h_n^{\,2}}}{h_1}$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{1}{n}\sum_{k=1}^{S}\cos(n\alpha_k)\right)^2}}{\sum_{k=1}^{S}\cos(\alpha_k)}$$

Therefore, output voltage THD of the presented waveform can be calculated. Theoretically, to get exact THD, infinite harmonics need to be calculated. However, it is not possible in practice. Therefore, certain number of harmonics will be given. It relies on how precise THD is needed.

## V. RESULT AND DISCUSSION

Simulation of various inverters using sinusoidal pulse width modulation was carried out with the help of "MATLAB ". Simulation was carried out to observe the improvement in the line voltage THD and Line current THD for RL load as the inverter level increases from 3-level and 5-level and 9 level .Following quantities have been observed.
1. Line voltage waveform
2. Line voltage waveform for RL load for three level inverter.
3. Line voltage waveform for RL load for five level inverter.
4. Substantial decrease in the THD as the frequency is increased.

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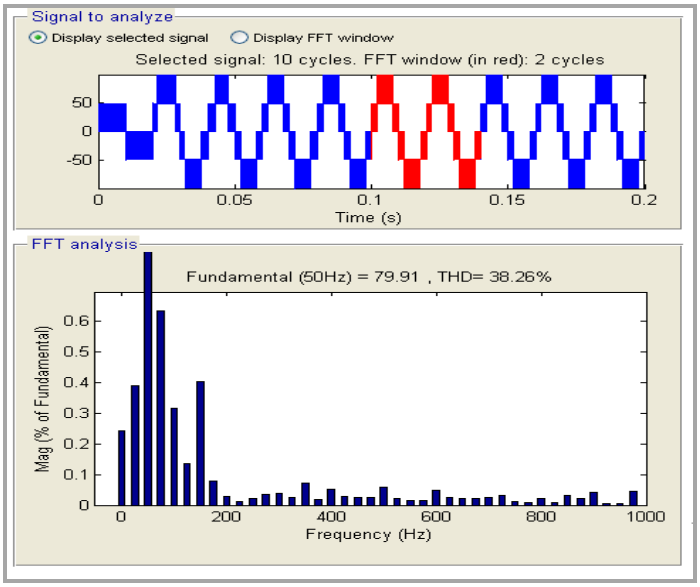


Figure 4: Harmonic spectrum Line Voltage of a 3-level inverter

From the above harmonic spectrum line voltage of a 3-level diode clamped multilevel inverter; it has been observed that the total harmonic distortion comes approx. 38.26%.Total Harmonic Distortion = 38.26%

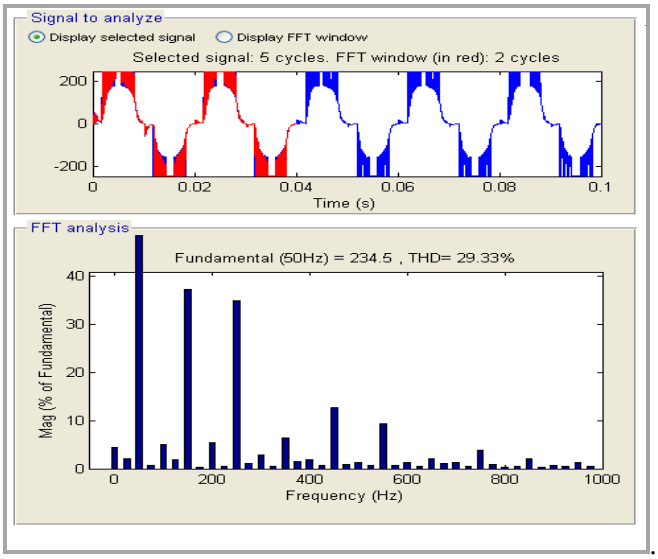


Figure 5: Harmonic spectrum Line Voltage of a 5-level inverter

From the above harmonic spectrum line voltage of a 5-level diode clamped multilevel inverter; it has been observed that the total harmonic distortion comes approx. 29.33%.Total Harmonic Distortion = 29.33%The simulation results obtained for a three level & five level multilevel verter as given below:-

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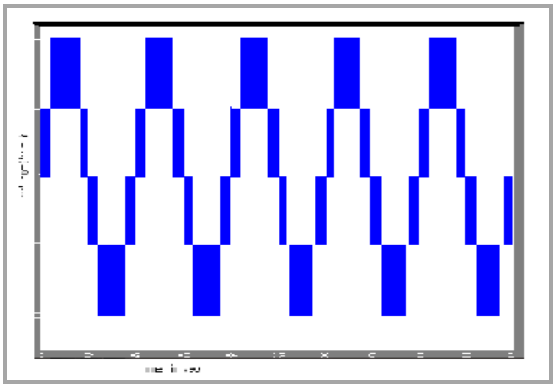

Figure 6: Output Voltage of a Three Level DCMI.

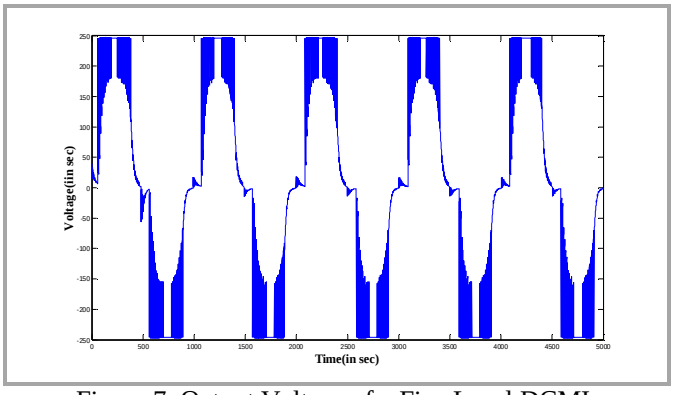


Figure 7: Output Voltage of a Five Level DCMI.

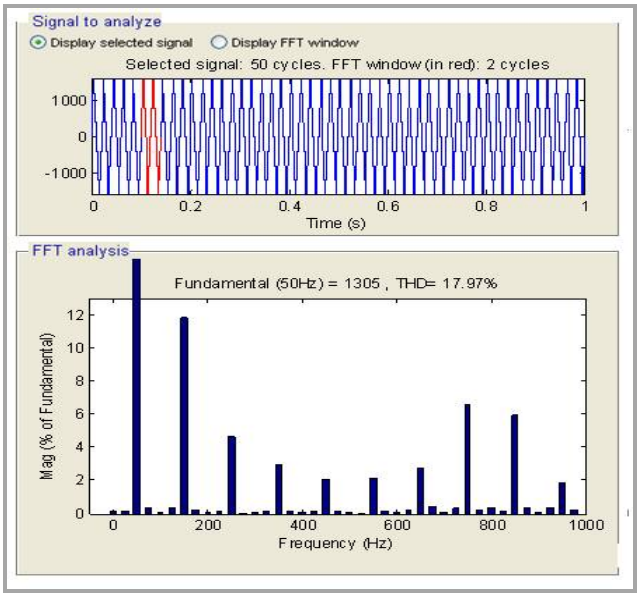


Figure 8: Harmonic spectrum Line Voltage of 9-level inverter.

From the above harmonic spectrum line voltage of a 9-level diode clamped multilevel inverter; it has been observed that the total harmonic distortion comes approx. 17.97%.

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## VI. CONCLUSION

The system represents an improved structure for large power conversion and may facilitate the practical application of the diode clamping inverter. A reduced switch diode clamped multilevel topology has been presented for drives application. The reduction in the number of switches, cost and complexity of the circuit makes it suitable for this application. It offer a low total harmonic distortion and high efficiency& are suitable for high voltages and high current application and also have higher efficiency because the devices has been switched at a lower frequency. The extensive simulation results validate the use of this multilevel inverter for drives application.

When using the 9-level, diode-clamp inverter controlled by modulation, the results shown that the output waveform were very similar to the sinusoidal wave comparing to the typical waveform, resulting to drive the load efficiently.

## Nomenclature

In Above Simulation Results:
**Figure 6 & 7** represents the variations in output voltage of a **3 & 5 level multilevel inverter** where
X axis-.Time in sec.
Y axis- Phase Voltage

$V_{dc}$- DC bus voltage.(between capacitor & switch)
DCMLI- Diode clamp multilevel inverter.
PWM- Pulse Width Modulation
THD- Total Harmonic Distortion

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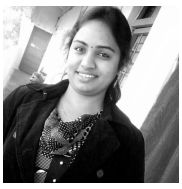

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